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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/758,802	01/15/2004	Dae-Woong Kang	8750-042	6500

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EXAMINER	
WARREN, MATTHEW E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 09/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/758,802	KANG ET AL.	
	Examiner	Art Unit	
	Matthew E. Warren	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *22-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-29 and 31-36* is/are rejected.

7)☒ Claim(s) *30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the Amendment filed on June 17, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 22-29 and 31-36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim et al. (US 6,642,105 B2).

The applied reference has a common inventor and assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claim 22, Kim et al. shows (fig. 32) a semiconductor device, comprising: a semiconductor substrate having a low voltage region (b) and a high voltage region (a); a first isolation layer (309 right) formed in the low voltage region and defining a first active

region (1b); a second isolation layer (309 left) formed in the high voltage region and defining a second active region (1a); a low voltage gate insulation (305b) layer formed on the first active region; and a high voltage gate insulation layer (305a) formed on the second active region and having a greater thickness than the low voltage gate insulation layer. A step region between the high voltage gate insulation layer and the second isolation layer has no recessed region and is spaced apart from a vertical axis passing through an edge corner of the second active region toward the second active region toward the second isolation layer adjacent to the vertical axis.

In re claim 23, Kim shows (fig. 32) a low voltage gate electrode (FG) formed on the low voltage gate insulation layer and disposed to cross over the first active region', and a high voltage gate electrode (313a) formed on the high voltage gate insulation layer and disposed to cross over the second active region.

In re claims 24 and 25, Kim discloses (col. 2, lines 44-50) that the low voltage region is a memory cell region. Kim shows in (fig. 31b) that the low voltage gate insulation layer is a tunnel oxide layer.

In re claim 26, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the second active region; a dummy gate electrode (317a) stacked on the main gate

electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

In re claim 27, Kim shows (fig. 32) that a thermal oxide (311) layer is interposed between the first isolation layer (309 right) and the semiconductor substrate, and between the second isolation layer (309 left) and the semiconductor substrate.

In re claim 28, Kim shows (fig. 32) that an edge region of the first isolation layer (307) is lower than a top surface of the low voltage gate insulation layer because the low voltage gate insulation layer (305b) is formed on top of the edge of the isolation trench.

In re claim 29, the Kim et al. shows (fig. 32) a semiconductor device comprising: a semiconductor substrate having a low voltage region (b) and a high voltage region (a); a first trench region (307 right) formed in the low voltage region to define a first active region (1b), the first active region having a protruded edge surface (the chunk of substrate 301 that is between the two adjacent trenches 309 in active region b); a first sloped region (sides of trench) interposed between the first trench region and the first active region, the first sloped region having a first incline that is downwardly extended from the protruded edge surface of the first active region; a second trench region (307 left) formed in the high voltage region to define a second active region (1a), the second active region having a relatively flat top surface; a second sloped region interposed between the second active region and the second trench region, the second sloped region (sides of trench) having a second incline that is downwardly extended from the

edge corner of the first active region; a first isolation layer filling (309 right) the first trench region and covering the first incline; a second isolation layer (309 left) filling the second trench region and covering the second incline; a low voltage gate insulation layer (305b) formed on the first active region, the low voltage gate insulation layer having a top surface lower than a top surface of the first isolation layer; a high voltage gate insulation layer (305a) formed on the second active region, the high voltage gate insulation layer having a flat top surface lower than a top surface of the second isolation layer and being thicker than the low voltage gate insulation layer, the top surfaces of the low voltage gate insulation layer and the high voltage gate insulation layer having a profile without any recessed regions.

In re claim 31, Kim shows (fig. 32) that a vertical axis passing through the edge of the top surface of the low voltage gate insulation layer is located in the first sloped region.

In re claim 32, as far as understood, Kim shows (fig. 32) that the low voltage gate insulation layer is formed on an upper corner of the first trench region.

In re claim 33, Kim shows (fig. 32) a low voltage gate electrode (FG) formed on the low voltage gate insulation layer and disposed to cross over the first active region', and a high voltage gate electrode (313a) formed on the high voltage gate insulation layer and disposed to cross over the second active region.

In re claims 34 and 35, Kim discloses (col. 2, lines 44-50) that the low voltage region is a memory cell region. Kim shows in (fig. 31b) that the low voltage gate insulation layer is a tunnel oxide layer.

In re claim 36, Kim shows (fig. 32) that a control gate electrode (CG) is formed over the low voltage gate insulation layer (305b), the control gate electrode crossing over the first active region; a floating gate (FG) is interposed between the control gate electrode and the low voltage gate insulation layer; a main gate electrode formed on the high voltage gate insulation layer, the main gate electrode (313a) crossing over the second active region; a dummy gate electrode (317a) stacked on the main gate electrode; and an inter-gate dielectric layer (315a) interposed between the floating gate and the control gate.

Allowable Subject Matter

Claim 30 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

Applicant's arguments with respect to claims 22-28 have been considered but are moot in view of the new ground(s) of rejection.

Applicant's arguments filed with respect to claims 29 and 31-36 have been fully considered but they are not persuasive. The applicant primarily asserts that Kim et al. does not disclose all of the elements of the claims, specifically the limitation of the protruded edge surface. The examiner believes that Kim et al. shows all of the elements of the claims including the limitation in question. As stated in the rejection

above, the examiner interprets the limitation of the protruded edge surface to be the portion of Kim's figure 32 that is the chunk of substrate 301 that is between the two adjacent trenches 309 in active region b. It is understood that the applicant intends to the protruded edge surface to be the portion of the semiconductor substrate that extends away from edge of the trench, however, the limitation as written is broad. When interpreted in the broadest possible manner, the protruded edge portion could be the chunk of substrate 301 that is between the two adjacent trenches 309 in active region a or b as stated in the rejection above. Therefore Kim shows all of the elements of the claims.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakamura et al. (US 5,783,491) shows (figs. 5D and 5E) a substrate having protruded edge portions, but such portions are taught to reduce the quality and reliability of the device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew E. Warren whose telephone number is (571) 272-1737. The examiner can normally be reached on Mon-Thur and alternating Fri 9:00-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

MEW

September 2, 2005

Tom Thomas

TOM THOMAS
SUPERVISORY PATENT EXAMINER